M2M OEM

8X32 v.2

MULTIPLEXED ARCHITECTURE

This multiplexed architecture 8x32 (v.2) provides an efficient and cost-effective solution to Original Equipment Manufacturers for integration into third-party systems. The board and dynamic-link libraries (dlls) are available.

Option 1: board without probe

Option 2: board with I-PEX connector

Option 3: board with Hypertronix connector

GENERAL	
L x W x H: 92mm x 65mm x 13mm	Weight: 51 g

HARDWARE CONFIGURATION
Multiplexed architecture: 8x32

LIBRARIES
dll provided

EMBEDDED PROCESSORS
Programmable FPGA

PULSERS	
Adjustable voltage: +/-10 to +/-50V with 1V step	Rise time < 10 ns (80V, 50 Ω)
Bipolar rectangular pulse, adjustable width: 20 ns to 1280 ns, step of 2.5 ns	Max. PRF: 30 KHz

RECEIVERS	
Bandwidth: 0,5Mhz – 20Mhz	Adjustable analog DAC on 36 dB (max. 40 dB/µs) synchronized on events
Adjustable gain from 0 to 90 dB	Cross-talk between two channels > 45 dB, max. input signal amplitude: 1 Vpp

DIGITIZER	
Max. sampling frequency: 100 MHz - Adjustable from 100 MHz to 6.6 MHz	Global delay: 0 up to 1.6 ms, step of 10 ns
Summed data resolution: 16 bits	Delay-laws at transmission/reception: 0 to 20 µs, step of 2.5 ns
Input impedance: 50 Ω | FIR filters	Digitizing depth: up to 50,000 samples (8,000 samples max. per elementary channel)

I/O	
3 encoders input, 1 external trigger input, 1 general purpose I-O	Option 1: board without probe connector
8 global TTL input, 8 global TTL output	Option 2: board with I-PEX connector
Powered by USB2	Option 3: board with Hypertronix connector

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